ACADEMIC REGULATIONS (R18PG)

COURSE STRUCTURE AND DETAILED SYLLABUS

For

M.Tech.- Regular Two Year Post Graduate Degree Programe

(Effective from 2018-19)

MASTER OF TECHNOLOGY

IN

EMBEDDED SYSTEMS AND VLSI

KANDULA SRINIVASA REDDY MEMORIAL COLLEGE OF ENGINEERING

(UGC-Autonomous)

Kadapa 516003, A.P

(Approved by AICTE, Affiliated to JNTUA, Ananthapuramu, Accredited by NAAC)

(An ISO 14001:2004 & 9001: 2015 Certified Institution)

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ABOUT THE COLLEGE

The college owes its existence to the keen interest of Late Kandula Obul Reddy to develop technical education in Rayalaseema region of Andhra Pradesh. With a view to translating his noble ideal of imparting technical education into reality, a Technical Training Institute at Vempalli, Kadapa District was started in 1979 under the aegis of Sri Kandula Obul Reddy charities. It is in the year 1980 that K.S.R.M. College of Engineering was established to perpetuate the memory of Late Sri. Srinivasa Reddy, youngest son of Late Sri Obul Reddy. Sri Srinivasa Reddy, a brilliantstudent of III year Mechanical Engineering at Delhi College of Engineering, New Delhi, met with his untimely death in a scooter accident on 18th Oct, 1979. The college was formally inaugurated on 14 November 1980 by Sri T. Anjaiah, the Chief Minister of Andhra Pradesh and it started functioning from the academic year 1980-81.

The college had its modest beginnings in 1980 with an intake of 160 students with core branches "Civil, Electrical & Electronics, Electronics & Communications and Mechanical Engineering. Keeping in view the latest trends, priorities and relevance in Engineering and Technology, the Board of Management decided to start Computer Science and Engineering in 1990 commemorating the decennial year of the college. With the conserted efforts of the Management and the Successive Principals, the departments have been strengthened year after year and the intake has steadily been increased to 1080 by the year 2014. Furthering its sphere of activity, the college started post graduate programme in CAD/CAM (ME), Geo-technical Engineering (CE) in the year 2004, Power Systems (EEE) & Computer Science and Engineering (CSE) during 2010-11 and Digital Electronics and Communication Systems (ECE) in 2011-12 respectively. The branches have constantly been strengthened by increasing the intake from time to time. This reflects one aspect of the progress and development of the college.

The College campus is located 7 K.M. away from Kadapa town on Kadapa to Pulivendula Highway in a calm and salubrious area of 35 acres. The College is set in a serene environment with lush greenery and fresh air. Four multi-storeyed RCC structures measuring 26,700 sqm provide accommodation for the departments. The College has dedicated electric power feeder and 250 KVA substation. Other capital resources include transport vehicles and four hostels. Excellent Bus facilities exist from Kadapa to Hyderabad, Vijayawada, Nellore, Tirupati, Kurnool, Bangalore, Chittoor and Chennai.

VISION

To evolve as center of repute for providing quality academic programs amalgamated with creative learning and research excellence to produce graduates with leadership qualities, ethical and human values to serve the nation.

MISSION

M1: To provide high quality education with enriched curriculum blended with impactful teaching learning practices.

M2: To promote research, entrepreneurship and innovation through industry collaborations.

M3: To produce highly competent professional leaders for contributing to Socio-economic development of region and the nation.

ABOUT THE DEPARTMENT

ECE Department was started in the year 1980 with an intake of 15. Since then the intake was gradually increased from 30 to 60 in the year 1990 then to 90 in the year 2001, to120 in the year 2007, to 180 in the year 2017. PG course with the specialization DECS was introduced in the year 2011 with an intake of 18 which was later increased to 18 in the year 2018and switched to Embedded Systems and VLSI in the year 2022.

The department has highly qualified and experienced faculty. There are Ten Doctorates in the department. The department has good infrastructural facilitates and is equipped with full-fledged laboratories. The department also has audio-visual facilities with four Digital Graphics Drawing Tablets for effective teaching. The staff members are deputed to participate in workshops, conferences, and refresher courses to keep in pace with recent developments in the field of Electronics & Communication Engineering.

The Department is accredited by AICTE-NBA twice. As part of the curriculum, Industrial visits are arranged for students of B. Tech (ECE) in III/IV year II Semesters. Students of our department actively participate in National-level Student Paper Presentation Contests being organized at various engineering colleges and universities. A few of them have been awarded in these paper presentation contests. The Department organizes the Co –Curricular and Extra Curricular activities through IEEE and IETE student chapters.

VISION

To emerge as globally recognized department in the frontier areas of Electronics and Communication Engineering.

MISSION

M1: To imbibe experiential, lifelong learning skills and problem solving capabilities through enriched curriculum and innovative teaching learning practices.

M2: To promote quality research by strengthening industry collaborations.

M3: To inculcate entrepreneurial attitude, leadership skills, human values and professional ethics.

PROGRAM EDUCATIONAL OBJECTIVES

PEO1: To apply the concepts of electronics, communication and computation and pursue career in core and allied industries to solve industrial and societal problems.
PEO2: To pursue higher education to progress professionally in contemporary Technologies and multidisciplinary fields with an inclination towards continuous learning.
PEO3: To exhibit professional skills, ethical values, interpersonal skills, leadership abilities, team spirit and lifelong learning.

PROGRAM OUTCOMES

PO1 - Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 - Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3 - Design/Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 - Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 - Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 - The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 - Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8 - Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of engineering practice.

PO9 - Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 - Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 - Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 - Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1: An ability to design electronic circuits for applications including signal processing, communications, computer networks, Embedded systems and in the field of VLSI

PSO2: Develop innovative technologies for Entrepreneurship with new cutting edge Technologies in the fields of electronic design, communication and automation.

PSO3: Identify and Apply Domain specific tools for Design, Analysis and Synthesis in the areas of Signal Processing, Communications, VLSI and Embedded systems.

KSRM College of Engineering, Kadapa-516003, AP
Regulations for PG Programs in Engineering (R18PG) (Effective from 2018-19)

Index

KSRM College of Engineering, Kadapa-516003, AP

Regulations for PG Programs in Engineering (R18PG)

1.0 Nomenclature

1.1 *Academic Term*: Extent of time during which academic instructions are initiated and completed.

1.2 *Academic Year*: Academic Term of, approximately, one year duration that usually starts in June/July and ends in April/May next

1.3 *Semester*: Either of two Academic Terms that make up an Academic Year

1.4 *Major*: A specific field of study

1.5 *Minor*: An area outside of, or complementary to, a Major

1.6 *Subject*: An area of knowledge that is studied as part of a Course

1.7 *Core*: A subject that is mandatory for a Major course of study

1.8 *Elective*: A subject that is selected for study to suit one's individual needs

1.9 *Audit Subject*: A subject that is studied to meet certain requirements but has no credits assigned to it

1.10 *Humanities subjects*: Subjects that describe and interpret human achievements, problems and historical changes at individual and societal levels covering the disciplines of literature, history, and philosophy

1.11 *Social Sciences subjects*: Subjects that describe the mental and behavioural activities of individuals, groups, organizations, institutions, and nations covering the disciplines of anthropology, economics, linguistics, political science, and psychology

1.12 *Exam*: A test to measure one's progress, knowledge, or ability in a subject

1.13 *Credit*: A numerical weight given to a subject

1.14 *Grade*: A numerical or alphabetic designation measuring the level ofachievement in an exam

1.15 *Attendance*: Physical presence of oneself in a classroom/laboratory forpurpose of a scheduled academic instruction

1.16 *Course*: A series of subjects that constitute a Major field of study

1.17 *Branch*: Same as Course

1.18 *Program*: Same as Course

1.19 *Specialization*: Same as branch

1.20 *Degree*: An academic title conferred to honour distinguished achievement

2.0 Short Title and Application

2.1 These rules and regulations may be called as R18

2.2 PG and come into force from Academic Year 2018-19 and exist until superseded by new regulations

2.3 These rules and regulations are applicable to all post graduate courses in engineering and technology leading to Master's Degree in Technology (M. Tech)

2.4 The Specializations offered, at present, are:

2.4.1 Geotechnical Engineering

2.4.2 Power Systems

2.4.3 Renewable Energy

2.4.4 Embedded System & VLSI

2.4.5 Artificial Intelligence & Data Science

2.5 The Institute may offer new Specializations in future to which these rules and regulations will be applicable

3.0 Suspension and Amendment of Rules

3.1 Academic Council has the authority to suspend a rule temporarily

3.2 Academic Council has the authority to amend a rule

3.3 For affirmative action on any suspension or amendment of a rule, an affirmative vote of three-fifths of the members present and voting shall be required in Academic Council

4.0 Requirements for Admission

4.1 At present, admissions into first semester of various Specializations are governed by Government and the Affiliating University. The eligibility criteria and procedure for admission are prescribed by Government andAffiliating University

4.2 A student is not allowed change of Specialization after admission

4.3 A student must fulfil medical standards required for admission

4.4 The selected students are admitted into first semester after payment of the prescribed fees

5.0 Structure of the M. Tech course

5.1 *Duration*: The duration of M. Tech degree course is four semesters

5.2 *Working Days*: Calendar for any semester shall be announced at least four weeks before its commencement. Minimum number of working days is 90 per semester

5.3 *Curriculum*: Each Specialization shall have core, elective and audit subjects. The curriculum for each Specialization shall be approved by its corresponding Board of Studies and then by the Academic Council

5.4 *Credits*: All subjects that are assessed for marks have credits assigned to them. The credits assigned to subjects shall be given in curriculum. The total number of credits for entire course is 68 for all Specializations. The distribution of total credits semester-wise is given in Table 1

Table 1 Semester-wise Total Credits

Semester	Total Credits
First Semester	18
Second Semester	18
Third Semester	16
Fourth Semester	16
Total for entire course	**68**

5.5 The curriculum and syllabus is given in Annexure-1 and Annexure-2 respectively

5.6 Responsibility and Advising: It is the responsibility of the student to understand and know the regulations and requirements to earn the degree. Each student admitted in to the degree programs is assigned to a Faculty Advisor who assists the student in designing an effective program of study. Students should consult their Faculty Advisors for selection of electives and for general advice on academic program.

6.0 Registration and Enrolment

6.1 Prior to opening of each semester, every student shall register for all the credit-bearing and audit subjects listed in curriculum of the semester. Excepting first semester, the registration for a semester shall be done during a specified week after end examinations of previous semester. In first semester, the registration shall be done within six working days from date of opening. Recommendation of Faculty Advisor is needed for registration

6.2 Late registration will be permitted with a fine, decided from time to time, up to six working days from the last date specified for registration

6.3 A student will be eligible for registration for a semester if she or he i) is promoted to that semester, ii) has cleared all fees to the Institute, library and hostel of previous semester, and iii) is not disqualified for registration by a disciplinary action of the Institute

6.4 A student will be enrolled and allowed to attend the classes on successful registration and payment of necessary fees to Institution, library, and hostel

6.5 Registration and enrolment will be controlled by the Office of the Controller of Examinations.

7.0 Assessment Procedure – Internal Tests and End Examinations

7.1 Performance of students in all subjects is assessed continuously through internal assessment tests and an End examination

7.2 Allocation of internal assessment and End examination marks

7.2.1 For theory subjects, the allocation is 40 marks for internal assessment and 60 marks for End examination totalling 100 marks

7.2.2 For laboratory/project work subjects, the allocation is 50 marks for

internal assessment and 50 marks for End examination totalling 100 marks

7.2.3 For mini-project/mini-project with seminar total 100 marks are allocated for internal assessment. There shall be no end examination for this mini-project

7.2.4 For all audit subjects the allocation is 40 marks for internal assessment and no allocation for End examination

7.3 Internal Assessment Examinations

7.3.1 Internal assessment means performance evaluation of students by faculty members who teach the subjects

7.3.2 For theory subjects, including audit subjects, the internal assessment shall be done by midterm tests. For each subject, two midterm tests will be conducted for 40 marks each and the internal assessment mark is the better of two marks. If any student abstains for any midterm test, she or he will be awarded zero marks for that midterm test. There shall be no choice of questions in midterm tests

7.3.3 For laboratory/practical subjects, the internal assessment will be based on regular laboratory work over full semester. The assessment will be done by the faculty concerned. The students shall be informed sufficiently early of the procedure to be followed for internal assessment

7.3.4 For subjects like seminar, project-work, industrial training, and comprehensive viva-voce, the internal assessment will be done by a concerned Department Committee consisting of two senior faculty members and faculty guide of concerned student. The assessment procedure will be informed sufficiently early to the students

7.4 End examinations

7.4.1 End examinations shall be conducted after completion of coursework in each semester

7.4.2 The question papers for theory subjects shall be set by faculty members outside of the Institute. The external faculty members for question paper setting will be selected by the Principal

7.4.3 Evaluation of answer scripts shall be done by faculty members from outside of the Institute selected by the Principal

7.4.4 For laboratory subjects, end examination shall be conducted by a committee consisting of two internal examiners. One examiner shall be recommended by Head of Department of concerned Major, and the other examiner shall be appointed by the Principal

7.4.5 For project work viva-voce, End examination shall be conducted by a committee consisting of one internal examiner, one external examiner, and the concerned guide of the student. Internal examiner shall be appointed by Head of Department of concerned Major, and the external examiner shall be appointed by the Principal

7.4.6 If a student abstains from End examination of any subject, for any reason, she or he shall be awarded zero marks in that subject

7.4.7 There is no end examination for audit subjects.

8.0 Method of Assigning Letter Grades and Grade Points

8.1 For all credit-bearing subjects, performance of a student in a subject is indicated by a letter grade that corresponds to absolute marks earned in that subject. Each letter grade is assigned a numeric Grade Point that is used to compute Grade Point Average on a scale of 0 to 10

8.2 Performance of a student in both internal assessment and End examination will be considered for awarding grades for credit bearing subjects. Total marks earned in a subject is the sum of marks obtained in internal and End examinations in that subject

8.3 Pass grade A+ to D+ is assigned to a subject based on total marks earned in that subject provided that a student earns at least i) 40% of marks in End examination marks and ii) 50% of marks in internal and End examination marks put together; otherwise fail grade F will be assigned to that subject

8.4 Grade I will be assigned to a subject if a disciplinary action is pending and is not resolved before publication of results. Office of Controller of Examinations shall resolve the pending disciplinary action within six working days from the date of publication of results and change the grade to any of A+ to D+ or F

8.5 Grade X will be assigned to a subject if a student abstains for End examination of that subject

8.6 The absolute marks and corresponding letter grade and grade points are given in Table2

Table 2 Letter Grades and Grade Points

Absolute Marks	Letter Grade	Grade Points	Remark
95-100	A+	10.0	Pass
90-94	A	9.5	Pass
85-89	A-	9.0	Pass
80-84	B+	8.5	Pass
75-79	B	8.0	Pass
70-74	B-	7.5	Pass
65-69	C+	7.0	Pass
60-64	C	6.5	Pass
55-59	C-	6.0	Pass
50-54	D+	5.5	Pass
0-49	F	0.0	Fail
-	I	0.0	Result Withheld
-	X	0.0	Absent for End Exam

8.7 *SGPA*: Semester Grade Point Average indicates the performance of a student in all credit-bearing subjects of a semester. SGPA is calculated as the weighted average of Grade Points of all subjects of the semester with corresponding credits of subjects as weights. Audit subjects are not considered for SGPA calculation

8.8 *CGPA*: Cumulative Grade Point Average indicates the performance of a student in all terms up to and including the current semester under consideration. CGPA is calculated as the weighted average of SGPAs with total credits in each semester as the weights

8.9 *Grade Card*: All students shall be issued Grade Cards after the publication of results of a semester. Grade Card is a statement of performance of a student in a semester. It contains information about each registered subject: type of subject, allocated credits, and letter grade earned. SGPA and CGPA will alsobe indicated.

9.0 Requirements for Completing Subjects

9.1 A student shall complete all credit-bearing and audit subjects successfully to be eligible for award of degree

9.2 *Credit-bearing subjects*: A student is considered to have completed a credit-bearing subject successfully and earned credits if she or he obtains a pass grade from A+ to D+ in that subject. If a student receives fail grade F or X in any subject, she or he must register for supplementary End examination for that subject as and when opportunity arises and improve grade to pass grade

9.3 *Audit subjects*: A student is considered to have successfully completed an audit subject if she or he earns at least 40% of marks in internal assessment marks.

Supplementary exam for audit subjects: If a student fails in audit subject, she or he shall register for supplementary examination in that subject as and when the opportunity arises and pass that subject. The supplementary exam will be conducted for 40 marks covering the entire syllabus and student is deemed to have passed in the subject if she or he earns 16 marks (40% marks) in the supplementary exam, disregard of her or his performance in internal tests.

10.0 Requirements for taking End Examinations

10.1 A student is eligible to take regular End Examinations of current semester ifshe or he full fills the attendance requirement

10.2 A student shall be promoted from current semester to succeeding semesteron satisfying the attendance requirement

10.3 A student shall complete all credit-bearing and audit subjects successfully before taking End examination for project viva-voce

10.4 Attendance Requirement

10.4.1 Attendance of students shall be recorded for credit-bearing and audit subjects as per the workload indicated in curriculum

10.4.2 Total class-periods conducted shall be reckoned from beginning toend of a semester as published in academic calendar

10.4.3 Aggregate Percentage of Attendance is calculated using total number of class-periods attended as numerator and total number of class- periods conducted for the concerned subject as the denominator

10.4.4 A minimum aggregate attendance of 75% is required for promotion to succeeding semester

10.4.5 A student can appeal to the Principal for condoning deficiency in aggregate attendance if she or he gets 65% or more aggregate attendance presenting a valid reason for deficiency. Such a student will be granted promotion if the Principal pardons the deficiency. Principal has the right to reject the appeal if it is not satisfied with the performance of the student or the reason cited for deficiency of the attendance

10.4.6 A student earning less than 75% aggregate attendance will be denied promotion. A student who is not promoted on basis of attendance shall be removed from the rolls and shall register for the same semester when opportunity arises. The current semester record of the student is cancelled automatically.

10.5 A student can forgo promotion and opt to repeat the current team on written request. Recommendation of the concerned Faculty Advisor is required for cancellation of promotion. This option shall be exercised before the commencement of the End Examinations of the current term.

11.0 Revaluation of End Examination Scripts

11.1 Revaluation of End Examination scripts is allowed for theory subjects only by paying requisite fee

11.2 A Procedure for Revaluation: The script will be revaluated by an examiner appointed by the Principal. The maximum of revaluation and regular end examination marks will be awarded for that subject

11.3 A student can apply for revaluation in a subject only once.

12.0 Supplementary End Examinations

12.1 Students are eligible to take Supplementary examinations in subjects with fail grade F or X only

12.2 Supplementary examinations for even semester subjects will be conducted with regular examinations of odd semester subjects and vice versa

12.3 A student will be allowed to improve grade in any theory subject provided she or he has completed coursework of all semesters but before award of provisional/final degree.

13.0 Requirements for Award of M. Tech degree

13.1 Time Limit for completion of requirements for award of degree is four calendar years from the date of admission. A student who could not complete all the requirements in this time limit shall forego admission and will be removed from the rolls of the Institute.

13.2 A student shall be eligible for award of degree provided she or he has:

13.2.1 Registered and successfully completed all required credit-bearing and audit subjects with a total of 68 credits

13.2.2 Secured a CGPA of 5.5 or more

13.2.3 Cleared all dues to the Institute, library and hostel

13.2.4 No disciplinary action is pending against her or him

13.2.5 Satisfied any other stipulation of the affiliating University

13.3 Award of Class: Each student will be given class in degree based on CGPA asgiven in Table 3

Table 3 Class of Degree

Class of Degree	Range of CGPA
Second Class	>= 5.5 but <6.5
First Class	>= 6.5 but <7.5
First Class with Distinction	>= 7.5

13.4 Consolidated Grade Card and Degree will issued under the seal of affiliating University

14.0 Transitory Regulations

14.1 A student who initially joins the Institute in a previous Regulation and has to re-join in any semester of the present Regulations, due to any reason, shall be bound by the rules of the current Regulations. Board of Studies of the concerned Major will specify, extra or otherwise, academic coursework to be undertaken by such students who re-join the current Regulations.

COURSE STRUCTURE

Department of ECE
M.Tech Embedded Systems and VLSI Course Structure

Semester-I									
S.No	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884101	RTL Simulation and Synthesis with PLDs	PC	3	0	0	40	60	3
2.	1884102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	40	60	3
3.	1884103	Research methodology and IPR	PC	2	0	0	40	60	2
4.	1884104 1884105 1884106 1884107	1. Parallel Processing 2. Digital Signal and Image Processing 3. VLSI signal processing 4. Design for testability	PE	3	0	0	40	60	3
5.	1884108 1884109 1884110 1884111	1. Programming Languages for Embedded Systems. 2. Micro-Electro Mechanical systems. 3. CAD of Digital System 4. CPLD, FPGA architectures and applications.	PE	3	0	0	40	60	3
6.	1884112	RTL Simulation and Synthesis with PLDs Lab	PC	0	0	4	50	50	2
7.	1884113	Microcontrollers and Programmable Digital Signal Processors Lab	PC	0	0	4	50	50	2
8.	1870A02	Disaster Management	AC				40		0
									18

Semester-II									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884201	Analog and Digital CMOS VLSI Design	PC	3	0	0	40	60	3
2.	1884202	Real Time Operating Systems	PC	3	0	0	40	60	3
3.	1884203 1884204 1884205 1884206	1. Memory Architectures 2. Advanced Computer Architecture 3. SoC Design 4. Low power VLSI Design	PE	3	0	0	40	60	3
4.	1884207 1884208 1884209 1884210	1. Communication Buses and Interfaces 2.Network Security and Cryptography 3.Physical design automation 4. Nanoelectronics	PE	3	0	0	40	60	3
5.	1884211	Analog and Digital CMOS VLSI Design Lab	PC	0	0	4	50	50	2
6.	1884212	Real Time Operating Systems Lab	PC	0	0	4	50	50	2
7.	1884213	Mini Project	PC	0	0	4	100	0	2
8.	1870A01	English for Research paper writing	AC				40		0
									18

Semester-III									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884301 1884302 1884303 1884304	1.IOT and its Applications 2. Hardware Software co-design 3.Artificial Intelligence 4. RFIC Design	PE	3	0	0	40	60	3
2.	1871305 1871306 1871307 1871308 1871309 1871310	Business Analytics Industrial Safety Operations Research Composite Materials Cost Management of Engineering Projects Waste to Energy	OE	3	0	0	40	60	3
3.	1884311	Dissertation Phase -I	Major Project	0	0	20	100	0	10
									16

Semester-IV									
S.No.	**Course Code**	**Course Name**	**Category**	**L**	**T**	**P**	**IM**	**EM**	**Credits**
1.	1884401	Dissertation Phase II	Major Project	0	0	32	50	50	Dissertation Phase II
									16

M.TECH.-I- SEMESTER SYLLABUS

Course Title	RTL SIMULATION AND SYNTHESIS WITH PLDS				M. Tech. ES &VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884101	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To introduce Verilog HDL for the design and functionality verification of a digital circuit.
- To understand the design of data path and control circuits for sequential machines
- To introduce the concept of realizing a digital circuit using PLDs

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the Static Timing Analysis and clock issues in digital circuits
CO 2	Appreciate the analysis of finite state machine of a controlling circuit
CO 3	Develop the Verilog HDL to design a digital circuit.
CO 4	Verify the functionality of the digital designs using PLDs.

UNIT I

Verilog HDL: Importance of HDLs, Lexical Conventions of Verilog HDL Gate level modeling: Built in primitive gates, switches, gate delays Data flow modeling: Continuous and implicit continuous assignment, delays Behavioral modeling: Procedural constructs, Control and repetition Statements,delays, function and tasks.

UNIT II

Digital Design: Design of BCD Adder, State graphs for control circuits, shift and add multiplier, Binary divider.FSM and SM Charts: Finite state diagram, Implementation of sequence detector using FSM, State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier.

UNIT III

ASIC Design Flow: Simulation, simulation types, Synthesis, synthesis methodologies, translation, mapping, optimization, Floor planning, Placement, routing, Clock tree synthesis, Physical verification.

UNIT IV

Static Timing Analysis: Timing paths, Meta-stability, Clock issues, Need and design strategies for multi- clock domain designs, setup and hold time Violations, steps to remove Setup and hold time violations.

UNIT V

Digital Design using PLD‟s: ROM, PLA, PAL- Registered PAL‟s, Configurable PAL‟s, GAL.CPLDs: Features, programming and applications using complex programmable logic devices. FPGAs: FieldProgrammable gate arrays Logic blocks, routing architecture, design flow.

Text Books:

1. Samir Palnitkar Verilog HDL,A Guide to “Digital Design and Synthesis”, 2nd Edition, 2003
2. Charles H. Roth “Fundamentals of Logic Design” , 5th Edition. Cengage Learning, 2010.
3. Bhasker J Verilog HDL Synthesis A Practical Primer, 1st edition, 1998
4. Modern Digital Electronics P Jain, 3rd Edition, TMH, 2003.
5. Data Sheets for CPLD & FPGA architectures, 1996.

Reference Books:

1. Donald D Givone, “Digital principles and Design”, TMH, 2016
2. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002.
3. Richard S. Sandige, “Modern Digital Design”, MGH, International Editions, 1990

Course Title	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS				M. Tech. ES&VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884102	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- To be able to identify and characterize architecture of Programmable DSP Processors
- To develop small applications by utilizing the ARM processor core and DSP processor based platform.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
CO 2	Identify and characterize architecture of Programmable DSP Processors
CO 3	Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration.

UNIT III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations. Code Composer Studio for application development for digital signal processing.

Text Books:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.

Reference Books:

1. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
3. Technical references and user manuals on www.arm.com.

Course Title	RESEARCH METHODOLOGY AND IPR				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884103	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		2	0	--	2	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand research problem formulation.
- To Analyze research related information
- To Follow research ethics
- To understanding that when IPR would take such important place in growth of individuals & nation,it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- To understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about,economic growth and social benefits.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand research problem formulation.
CO 2	Analyze research related information
CO 3	Follow research ethics
CO 4	Apply Patent Rights in filing.
CO 5	Describe new developments in IPR.

UNIT I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT II

Effective literature studies approaches, analysis Plagiarism and Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies,IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd , 2007.

Reference Books:

1. Mayall, "Industrial Design", McGraw Hill, 1992.
2. Niebel, "Product Design", McGraw Hill, 1974.
3. Asimov, "Introduction to Design", Prentice Hall, 1962.
4. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
5. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Course Title	PARALLEL PROCESSING				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884104	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To overview of the architectures and communication networks employed in parallel computers.
- The course covers the foundations for development of efficient parallel algorithms, including examples from relatively simple numerical problems, sorting, and graph problems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand parallel processing and pipelining techniques.
CO 2	Identify limitations of different architectures of computer
CO 3	Analysis quantitatively the performance parameters for different architectures
CO 4	Investigate issues related to compilers and instruction set based on type of architectures
CO 5	Develop parallel programming techniques.

UNIT I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT II

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT III

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT IV

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

UNIT V

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

Text Books:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2. Kai Hwang, "Advanced Computer Architecture", TMH
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.

Reference Books:

1. William Stallings, "Computer Organization and Architecture, Designing for performance "Prentice Hall, Sixth edition
2. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing", MGH
3. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan

Course Title	**DIGITAL SIGNAL AND IMAGE PROCESSING**					**M. Tech. ES & VLSI I Sem**		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
1884105	**PE**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**			

Course Objectives:

- To study the discrete time signals and system in various domains
- To learn the concepts of design of digital filtering
- To study different image enhancement, Restoration and compression techniques
- To understand image segmentation algorithms

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Analyze discrete-time signals and systems in various domains(i.e. Time, Z and Fourier)
CO 2	Design the digital filters (both IIR and FIR)from the given specifications.
CO 3	Analyzethequantizationeffectsindigitalfiltersandunderstandthebasicsofimagesampling, quantization and image transforms.
CO 4	Understand the concepts of image enhancement, image restoration, image segmentation and Color Image processing.
CO 5	Analyze various image compression techniques.

UNIT I

Review of Discrete Time signals and systems, Characterization in time, Z and Fourier domain, Fast Fourier Transform using Decimation In Time (DIT) and Decimation In Frequency (DIF) Algorithms.

UNIT II

IIR Digital Filters: Introduction, Analog filter approximations–Butterworth and Chebyshev, Design of IIR Digital filters from analog filters using Impulse Invariance, Bilinear Transformation methods.
FIR Digital Filters: Introduction, Design of FIR Digital Filters using Window Techniques, Frequency Sampling technique, Comparison of IIR &FIR filters.

UNIT III

Analysis Of Finite Word length Effects: The Quantization Process and Errors, Quantization of Fixed-Point Numbers, Quantization of Floating- Point Numbers ,Analysis of Coefficient Quantization effects.
Introduction To Digital Image Processing: Introduction, components in image processing system, Applications of Digital image processing, Image sensing and acquisition, Image sampling, Quantization, Basic Relationships between pixels, ImageTransforms:2D-DFT, DCT, Haar Transform.

UNIT IV

Image Enhancement: Intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, the basics of filtering in the frequency domain, image smoothing using frequency domain filters, Image Sharpening using frequency domain filters ,Selective filtering.

Image Restoration: Introduction, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering.
Image Segmentation: Fundamentals, point, line, edge detection, thresholding, and region based segmentation.

UNIT V

Image Compression: Fundamentals, Basic compression methods: Huffman coding, Arithmetic coding, Run-Length coding, Block Transform coding, Predictive coding, Wavelet coding.

Color Image Processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

Text Books:

1. JohnG.Proakis,DimitrisG.Manolakis,"DigitalSignalProcessing",Principles,Algorithms,andApplications,PearsonEducation/PHI,2007.
2. S.K.Mitra."DigitalSignalProcessing–AComputerbasedApproach",TMH,3rdEdition,2006
3. RafaelC.Gonzalez and Richard E.Woods,"Digital Image Processing", PearsonEducation,2011.
4. S.Jayaraman,Esakkirajan,Veerakumar,"DigitalImageProcessing",McGrawHillPublishers,2009

Reference Books:

1. Andreas Antoniou,"Digital Signal Processing", TATAMcGrawHill, 2006
2. MHHayes, DigitalSignalProcessing, Schaum"sOutlines, TATAMc-GrawHill, 2007.
3. AnilK.Jain,"Fundamentals of Digital Image Processing" ,PrenticeHall ofIndia,2012.

Course Title	VLSI SIGNAL PROCESSING				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884106	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the static, small signal and large signal modeling of MOS Transistor.
- To understand the DSP architectures.
- To understand the operation of design aspects of processors.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Ability to modify the existing or new DSP architectures suitable for VLSI.
CO 2	Understand the concepts of folding and unfolding algorithms and applications.
CO 3	Analyze to implement fast convolution algorithms.
CO 4	Develop Low power design aspects of processors for signal processing and wireless applications.

UNIT I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT II

Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems

Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT V

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design .Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Text Books:

1. Keshab K. Parthi[A1] , "VLSI Digital signal processing" systems, design and implementation[A2] , Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", McGraw Hill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.

Course Title	DESIGN FOR TESTABILITY				M. Tech. ES &VLSI		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884107	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To analyze the digital circuits with the presence of faults.
- To generate the test patterns.
- To understand the concept of controllability and observability.
- To determine the built in self test.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Design digital circuits including various levels of modeling and different approaches for simulation.
CO 2	Analyze the digital circuits with the presence of faults and evaluation of given test set for fault coverage.
CO 3	Create test patterns for detecting single stuck faults in combinational and sequential circuits.
CO 4	Explain controllability and observability and schemes for introducing testability into digital circuits which will make circuits more testable with ease and improve fault coverage.
CO 5	Determine built in self test (BIST) and different approaches for introducing BIST into logic circuits memories and embedded cores.

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals. Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling. Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level. Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Text Books:

1. Miron Abramovici, Melvin A. Breur, Arthur D. Friedman, “Digital Systems Testing and Testable Design”, Jaico Publishing House, 2001.
2. Alfred Crouch., “Design for Test for Digital ICs & Embedded Core Systems”, Prentice Hall.
3. Robert J. Feugate, Jr., Steven M. Mentyn, “Introduction to VLSI Testing”, Prentice Hall, Englehood Cliffs, 1998.

Course Title	PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEM				M. Tech. ES &VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884108	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To explore the difference between general purpose programming languages and Embedded Programming Language.
- To provide case studies for programming in embedded systems.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Expected to learn the basics of Embedded C with reference to 8051.
CO 2	Understand how to handle control and data pins at hardware level.
CO 3	Capable of introducing into objective nature of Embedded C.
CO 4	Understand the specifications of real time embedded programming with case studies

UNIT I

Programming Embedded Systems in C Introduction, What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions

Introducing the 8051 Microcontroller Family

Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions.

UNIT II

Reading Switches Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT III

Adding Structure to your Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

UNIT IV

Meeting Real-Time Constraints Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.

UNIT V

Case Study: Intruder Alarm System Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions.

Text Books:

1. Michael J. Pont "Embedded C", A Pearson Education.

Reference Books:

1. PIC micro MCU C-An introduction to programming, The Microchip PIC in CCS C By

Course Title	MICRO-ELECTRO MECHANICAL SYSTEMS.				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884109	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- Able to know a new and upcoming interdisciplinary area.
- To understand generating better electronic gadgets
- Able to know technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices
- To understand a new stream of Electronics-MEMTRONICS.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	A new and upcoming interdisciplinary area.
CO 2	Generating better electronic gadgets
CO 3	Technologies involving miniaturized Electrical, Mechanical and Electro-mechanical devices
CO 4	A new stream of Electronics-MEMTRONICS

UNIT I

Introduction, Basic Structures of MEM Devices – (Canti Levers, Fixed Beams diaphragms). Broad Response of MEMS to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatibility of MEMS with VLSI Applications in Electronics, Broad Advantages and Disadvantages of MEMS from the point of Power Dissipation, Leakage etc.

UNIT II

Review of Mechanical Concepts like Stress, Strain, Bending Moment, and Deflection Curve. Differential equations describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with voltage in C.L, Deflection Vs Voltage Curve, Critical Deflection, Description of the above w.r.t. Fixed Beams. Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT III

Two Terminal MEMS – capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT IV

MEM Circuits & Structures for Simple GATES – AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT V

MEM Technologies: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

Text Books:

1. Gabriel.M. Reviez, R.F." MEMS Theory", Design and Technology, Thon Wiley & Sons, 2003.
2. Thimo Shenko, "Strength of Materials", CBS Publishers & Distributors.
3. K. Pitt, M.R. Haskard, "Thick Film Technology and Applications", 1997.

Reference Books:

1. Wise K.D. (Guest Editor), "Special Issue of Proceedings of IEEE", Vol.86, No.8, Aug 1998.
2. Ristic L. (Ed.) Sensor Technology and Devices, Artech House, London 1994

Course Title	CAD OF DIGITAL SYSTEMS					M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884110	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To understand the fundamentals of CAD tools for modeling, design, test and verification of VLSI Systems.
- To study various phases of CAD, including simulation, physical design, test andVerification.
- To be able to demonstrate the knowledge of computational algorithms and tools for CAD.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems.
CO 2	Understand various phases of CAD, including simulation, physical design, and test andverification.
CO 3	Demonstrate knowledge of computational algorithms and tools for CAD.

UNIT I

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules Layout of Basic Devices, Fabrication Process and its Impact on Physical Design, Scaling Methods, Status ofFabricationProcess, Issues related to the Fabrication Process, Future of Fabrication Process, Solutions for Interconnect Issues, Tools for Process Development.

UNIT II

VLSI design automation tools – Data Structures and Basic Algorithms, Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, graph theory and Computational complexity, tractable and intractable problems.

UNIT III

General purpose methods for combinational optimization – Partitioning- Problem Formulation ,Classification of Partitioning Algorithms, Group Migration Algorithms , Simulated Annealing Simulated Evolution, Other Partitioning Algorithms Performance Driven Partitioning Floor planning- Chip planning, Pin Assignment , Integrated Approach, Placement- Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms , Partitioning Based Placement Algorithms, Performance Driven Placement, Routing -Global Routing,Problem Formulation,Classification of Global Routing Algorithms, Maze Routing Algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms. Steiner Tree based Algorithms Integer Programming Based Approach, Performance Driven Routing.

UNIT IV

Simulation- Gate-level Modelling and Simulation, Switch-level Modeling and Simulation, Logic Synthesis and Verification - Introduction to Combinational Logic Synthesis , Binary-decision Diagrams, Two-level Logic Synthesis, High-level Synthesis- Hardware Models for High level Synthesis , Internal Representation of the Input Algorithm , Allocation, Assignment and Scheduling.

UNIT V

MCMs-VHDL-Verilog-implementation of adders, subtractors, multiplexers, Demultiplexers and counters using VHDL.

Text Books:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".

2. S.H. Gerez, "Algorithms for VLSI Design Automation".

Course Title	CPLD, FPGA ARCHITECTURS AND APPLICATIONS.				M. Tech ES & VLSI I Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884111	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	0	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- Implement given task using FPGA
- Develop test pattern to test the FPGA
- Design a product level approach utilizing FPGAs.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Differentiate between ROM,PAL,PLA,SPLD,CPLD,FPGA
CO 2	Compare the features of Various CPLDs in terms of their architecture, Logic blocks
CO 3	Compare the features of Various FPGAs in terms of their Architecture, Configurable logic block and routing.
CO4	Gain knowledge on routing algorithms adopted in FPGAs.
CO5	Test a particular PLD using various techniques like design validation, Timing verification.

UNIT I

Programmable logic: Programmable read only memory (prom), Programmable Logic Array (PLA), Programmable Array Logic (PAL). Sequential Programmable Logic Devices (SPLDs). Programmable Gate Arrays (PGAs), CPLD and FPGA, design flow using FPGA, programming technologies.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Logic cells and features of commercially available FPGA's- XILINX XC4000, Virtex-II FPGA's, XILINX SPARTAN II, Alteras Act1, Act2, Act3 FPGA's, Actel FPGA's, AMD FPGA.

UNIT III

CPLD's: complex programmable logic devices, logic block, I/O block, interconnect matrix, logic blocks and features of Altera flex logic 10000 series CPLD's , max 7000 series CPLD's, AT & T – ORCA's (Optimized Reconfigurable Cell Array), Cypres flash 370 device technology, lattice PLSI's architectures.

UNIT IV

Placement: objectives, placement algorithms: Mincut-Based placement, iterative improvement placement, simulated annealing. Routing: objectives, segmented channel routing, Maze routing, Routability estimation, Net delays, computing signal delay in RC tree networks.

UNIT V

Digital Front End and back End tools for FPGAs & ASICs, FPGA implementation steps .Verification: introduction, logic simulation, design validation, timing verification .Testing concepts: failures, mechanisms and faults, fault coverage, ATPG methods, and programmability failures.

Text Books:

1. P.K. Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Pearson Education 2009.
2. S. Trimberger, Edr, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
3. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S. Brown, R. Francis, J. Rose, Z.Vransic, Field Programmable Gate array, Kluwer Publn, 1992. Manuals from Xilinx, Altera, AMD, Actel.

Course Title	**RTL SIMULATION AND SYNTHESIS WITH PLDS LAB**				**M. Tech. ES &VLSI I Sem**		
Course Code	**Category**	**Hours/Week**			**Credits**	**Maximum Marks**		
1884112	**PC**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		--	--	4	2	50	50	100
						End Exam Duration: 3Hrs		

Course Objectives:

- To implement the Verilog code for combinational and sequential circuits.
- To implement the Verilog code for Discrete Fourier Transform/FFT algorithm
- To design FSM, Vending Machine.

Course Outcomes: On successful completion of this course, the students will be able to	
CO 1	To design various combinational and sequential circuits.
CO 2	To design FSM machines, Vending machines.
CO 3	Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
CO 4	Realize single port SRAM in Verilog
CO 5	Implement UART/USART in Verilog.

LIST OF EXPERIMENTS:

1. Verilog implementation of 8:1 Mux/Demux,
2. Verilog implementation of Full Adder, 8-bit Magnitude comparator.
3. Verilog implementation of 3-bit Synchronous Counters.
4. Verilog implementation of Parity generator.
5. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
6. Vending machines - Traffic Light controller, ATM, elevator control.
7. PCI Bus & arbiter and downloading on FPGA.
8. UART/ USART implementation in Verilog.
9. Realization of single port SRAM in Verilog.
10. Verilog implementation of Arithmetic circuits like serial adder/ subtractor.
11. Verilog implementation of paralleladder/subtractor, serial/parallel multiplier.
12. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

<table>
<tr><td>Course Title</td><td colspan="5">MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB</td><td colspan="3">M. Tech. ES & VLSI I Sem</td></tr>
<tr><td>Course Code</td><td>Category</td><td colspan="3">Hours/Week</td><td>Credits</td><td colspan="3">Maximum Marks</td></tr>
<tr><td rowspan="2">1884113</td><td rowspan="2">PC</td><td>L</td><td>T</td><td>P</td><td>C</td><td>Continuous Internal Assessment</td><td>End Exams</td><td>Total</td></tr>
<tr><td>-</td><td>--</td><td>4</td><td>2</td><td>50</td><td>50</td><td>100</td></tr>
<tr><td colspan="5"></td><td colspan="4">End Exam Duration: 3Hrs</td></tr>
<tr><td colspan="9">Course Objectives:
• To understand, compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
• To be able to identify and characterize architecture of Programmable DSP Processors
• To develop small applications by utilizing the ARM processor core and DSP processor based platform.</td></tr>
<tr><td colspan="9">Course Outcomes: On successful completion of this course, the students will be able to</td></tr>
<tr><td>CO 1</td><td colspan="8">Install, configure and utilize tool sets for developing applications based on ARM processor Core SoC and DSP processor.</td></tr>
<tr><td>CO 2</td><td colspan="8">Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.</td></tr>
</table>

LIST OF ASSIGNMENTS:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6748 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

Course Title	DISASTER MANAGEMENT (Audit Course)				M. Tech. ES & VLSI I Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1870A02	Audit Course	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		2	0	0	0	40	--	40
Mid Exam Duration: 2 Hours								

Course Objectives:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand foundations of hazard, disasters and natural/social phenomena.
CO 2	Analyze Repercussions of disasters and hazards.
CO 3	Understand key concepts in disaster risk reduction and humanitarian response.

UNIT I

Introduction to Disaster: Definition, Factors and Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

UNIT II

Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III

Disaster Prone Areas In India

Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

UNIT IV

Disaster Preparedness and Management

Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk:

Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

UNIT V

Risk Assessment

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People'sParticipation In Risk Assessment. Strategies for Survival.

Disaster Mitigation

Meaning, Concept and Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

Text Books:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.

Reference Books:

1. Fundamentals of Disaster Management, Shekhawat R.S, Bhatnagar Harshul.
2. Disaster management, Ruthra, Lakshmi Publications.
3. Disaster Management and Preparedness, Nidhi Gauba Dhawan, Ambrina Sardar Khan, CBS Publishers.

M.TECH.-II- SEMESTER SYLLABUS

Course Title	ANALOG AND DIGITAL CMOS VLSI DESIGN				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884201	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Combinational MOS logic circuits, and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Appreciate the trade-offs involved in analog integrated circuit design.
CO 2	Understand and appreciate the importance of noise and distortion in analog circuits.
CO 3	Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
CO 4	Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, Alternative CMOS Logics, Estimation of Delay and Power, Adders Design.
CO 5	Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

Digital CMOS Design:

UNIT I

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

UNIT II

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.

Combinational logic: Static CMOS design, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT III

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design

UNIT IV

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gatestage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT V

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise. Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP.

Text Books:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Reference Books:

1. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
2. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
3. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
4. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Course Title	REAL TIME OPERATING SYSTEMS				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884202	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To emphasize on the concept of a complete system consisting of asynchronous interactions between concurrently executing hardware components and device driver software in order to illustrate the behavior of a computer system as a whole.
- To understand and design RT Linux and Embedded Linux

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the advanced concepts of computer architecture. Exposing the major differentials of RISC and CISC architectural characteristics.
CO 2	Able to investigate modern design structures of Pipelined and Multiprocessors systems.
CO 3	Able to become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

UNIT I

INTRODUCTION: Introduction to UNIX/LINUX, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT II

REAL TIME OPERATING SYSTEMS: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency. Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT III

OBJECTS, SERVICES AND I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT IV

EXCEPTIONS, INTERRUPTS AND TIMERS: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT V

CASE STUDIES OF RTOS: RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

Text Books:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011

Reference Books:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

Course Title	MEMORY ARCHITECTURES				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884203	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the architecture and design semiconductor memory circuits and subsystems

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Select architecture and design semiconductor memory circuits and subsystems.
CO 2	Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO 3	Know how the state-of-the-art memory chip design

UNIT I

Random Access Memory Technologies:

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers

UNIT III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT IV

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing

UNIT V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues.

Text Books:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs andApplications", Wiley Inter science
2. KiyooItoh, "VLSI memory chip design", Springer International Edition

Reference Books:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI

Course Title	ADVANCED COMPUTER ARCHITECTURE				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884204	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To Understand the advanced concepts related to computer architecture and storage systems, parallelism and pipelining concepts, the design aspects and challenges

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the advanced concepts related to computer architecture and storage systems.
CO 2	Understand parallelism and pipelining concepts, the design aspects and challenges.
CO 3	Analyze the high performance scalable Multithreaded and multiprocessor systems.

UNIT I

Fundamentals of Computer Design: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

Instruction Set Principles and Examples: classifying instruction set- memory addressing- type and size of operands- addressing modes for signal processing operations in the instruction set, instructions for control flow, encoding an instruction set, the role of compiler.

UNIT II

Instruction Level Parallelism (ILP): overcoming data hazards reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP.

ILP Software Approach: compiler techniques- static branch protection, VLIW approach, H.W support for more ILP at compile time- H.W verses S.W solutions.

UNIT III

Memory Hierarchy Design: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT IV

Multiprocessors and Thread Level Parallelism: Symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT V

Storage Systems- Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

Interconnection Networks and Clusters: Interconnection network media, practical issues in interconnecting networks- examples, clusters, designing a Cluster.

Text Books:

1. Computer Architecture A quantitative approach 3rd edition John L. Hennessy & David A. Patterson Morgan Kufmann (An Imprint of Elsevier)

Reference Books:

1. Kai Hwang and A.Briggs "Computer Architecture and parallel processing", International Edition McGraw-Hill.
2. Kai Hwang, "Advanced Computer Architecture", McGraw Hill Education,1993.
3. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

Course Title	SoC DESIGN					M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884205	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- The Objective of this course is to provide the students with knowledge about the system architecture and components.
- To understand the SoC process and its memory design.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Identify and formulate a given problem in the frame work of SoC based design approaches for engineering applications
CO 2	Realize impact of SoC on electronic design philosophy and Macro-electronics there by incline towards entrepreneurship & skill development
CO 3	Compute different simulation models
CO 4	Analyze the power optimization for digital systems
CO 5	Understand the importance of synthesis

UNITI

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NIS C approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

UNIT II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems,SoCrelatedmodelingofdatapathdesignandcontrollogic,Minimizationofinterconnectsimpact,clocktreedesign issues.

UNITIV

Low power SoC design / Digital system: Design synergy, Low power system perspective-power gating, clock gating, and adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V

Synthesis Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multicore systems, darksiliconissues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Text Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.

2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

Reference Books:

1. Rochit Rajsuman,"System-on-a-chip:Design and test", Advan testAmerica R&D Center,2000
2. P Mishra and NDutt,"Processor Description Languages",MorganKaufmann,2008
3. MichaelJ.FlynnandWayne Luk, "ComputerSystemDesign:System-on-Chip".Wiley

Course Title	LOW POWER VLSI DESIGN				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884206	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- Study different abstraction levels in VLSI Design and the impact of power reduction methods at higher levels
- Apply leakage control mechanisms to reduce static power consumption in DSM VLSI regime
- Apply technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits
- Study and apply various software power estimation and optimization techniques for low power VLSI system design
- Apply low power circuit and architectural techniques for reducing power consumption in SRAM designs

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	**Distinguish** the impact of various power reduction techniques at different levels of VLSI Design.
CO 2	**Identify** the sources of power dissipation and apply leakage control techniques to reduce static power consumption in CMOS circuits.
CO 3	**Apply** technology independent and technology-dependent techniques for Dynamic power reduction in CMOS circuits
CO 4	**Analyze** different power reduction techniques for VLSI systems at Design time, Run-time and Stand-by modes.
CO 5	**Employ** software power estimation and optimization methods for low power VLSI system design.

UNIT I

Introduction to Low Power design: SOC levels, Emerging zero-power applications (WSN), Design-productivity challenge, Impact of implementation choices, Motivation for LPD, Basic VLSI Design Flow, Optimization examples at various levels (System, Sub-system, RTL, Gate, Circuit and Device levels). Sources of power dissipation, MOS transistor leakage components, Static Power dissipation, Active Power dissipation, Circuit Techniques for Low Power Design

UNIT II

Power Optimization Techniques – I: Dynamic Power Reduction Approaches, Circuit Parallelization, Voltage Scaling Based Circuit Techniques, Circuit Technology – Independent Power Reduction, Circuit Technology Dependent Power Reduction; Leakage Power Reduction – Leakage Components, Design Time Reduction Techniques, Run-time Stand-by Reduction Techniques, Run-time Active Reduction Techniques Reduction in Cache Memories.

UNIT III

Power Optimization Techniques – II: Low Power Very Fast Dynamic Logic Circuits, Low Power Arithmetic Operators, Energy Recovery Circuit Design, Adiabatic – Charging Principle and its implementation issues.

Software Design for Low Power: Sources of Software Power Dissipation, Software Power Estimation, Software Power Optimizations, Automated Low-Power Code Generation, Co-design for Low Power.

UNIT IV

Low Voltage Low Power Static Random Access memories: Basics, Race between 6T and 4T memory cells, LVLP SRAM Cell designs- Shared bit-line SRAM cell configuration, Power efficient 7T SRAM cell with current mode read and write, The 1T SRAM cell, Pre-charge and Equalization Circuit, Dynamic and static decoders, Voltage Sense amplifier, Output Latch,

Low Power SRAM Techniques: Sources of SRAM Power, Low Power Circuit techniques such as capacitance reduction, Leakage current reduction.

UNIT V

Large LP VLSI System design and Applications: Architecture-driven Voltage Scaling, Power optimization using operation reduction and operation substitution, Pre-computation based optimization, Multiple and Dynamic supply voltage design, Choice of supply voltages, varying the clock speed, varying the VDD of RAM structures, Gated Clocking. Leakage current reduction in medical devices (Ref-1)

Text Books:

1. Kiat-Seng Yeo and Kaushik Roy, “Low-Voltage, Low-Power VLSI Subsystems, Tata McGrawhill Edition, 2005. (Units I, IV and V)
2. Christian Piguet, “Low Power CMOS Circuits Technology, Logic Design and CAD Tools”, 1st Indian Reprint, CRC Press, 2010.(Units II and III)
3. Kaushik Roy and Sharat Prasad, “ Low-Power CMOS VLSI Circuit Design” , Wiley Pub., 2000 (Unit III)

Reference Books:

1. DimitriosSoudris, Christian Piguet and CoastasGoutis, “Designing CMOS Circuits for Low Power”, Kluwer Academic Pub, 2002
2. J. Rabaey, Low Power Design Essentials, 1st Edition, Springer Publications, 2010

Course Title	COMMUNICATION BUSES AND INTERFACES				M. Tech. ES & VLSI II Sem		
Course Code	**Category**	**Hours/Week**		**Credits**	**Maximum Marks**		
1884207	**PE**	**L**	**T**	**P**	**C**	**Continuous Internal Assessment**	**End Exams**	**Total**
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					**End Exam Duration: 3Hrs**		

Course Objectives:

- To Develop APIs for configuration, reading and writing data onto serial bus.
- To learn how to select a particular serial bus suitable for a particular application

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Select a particular serial bus suitable for a particular application.
CO 2	Develop APIs for configuration, reading and writing data onto serial bus.
CO 3	Design and develop peripherals that can be interfaced to desired serial bus.

UNIT I

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate,features Limitations and applications of RS232, RS485, I^2C , SPN

UNIT II

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers-Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT III

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, isochronous transfer. Enumeration- Device detection, Default state, addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor,String descriptor. Device driver.

UNIT V

Data streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) configurations,Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Text Books:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2 Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- JanAxelson, Lakeview Research, 2nd Ed.,

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2 PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press

Course Title	NETWORK SECURITY AND CRYPTOGRAPHY				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884208	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the security & number theory.
- To learn about Key Distribution and Management, Diffie-Hellman Key Exchange.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Identify and utilize different forms of cryptography techniques.
CO 2	Incorporate authentication and security in the network applications.
CO 3	Distinguish among different types of threats to the system and handle the same.

UNIT I

Security & Number Theory: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques. Introduction, Fermat‟s and Euler‟s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT II

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT III

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms:MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT IV

Authentication: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

UNIT V

System Security: Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, VirusCountermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

Text Books:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", PearsonEducation, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communicationin a Public World", Prentice Hall, 2nd Edition

Reference Books:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "InsideNetwork Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013

Course Title	PHYSICAL DESIGN AUTOMATION				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884209	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To Understand the relationship between design automation algorithms and Various constraints posedby VLSI fabrication and design technology.
- To Identify layout optimization techniques and map them to the algorithms.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the relationship between design automation algorithms and Various constraints posedby VLSI fabrication and design technology.
CO 2	Adapt the design algorithms to meet the critical design parameters.
CO 3	Identify layout optimization techniques and map them to the algorithms
CO 4	Develop proto-type EDA tool and test its efficacy

UNIT I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multi-chip modules. Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost.

UNIT II

Factors, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms.

UNIT III

Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbour pointers, corner stitching, multi-layer operations.

UNIT IV

Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum colouring, maximum k-independent set algorithm, algorithms for circle graphs.

UNIT V

Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms.

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical DesignAutomation, CRC Press, 2008

Course Title	NANO ELECTRONICS					M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884210	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To study the basics of electronics, transistors.
- To Understand the band structure models
- To Understand the nano capacitors, coulomb blockade

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To know nano electronics holds the capacity for mass production of high-quality nano devices with an enormous variety of applications.
CO 2	Design the scaling of transistors.
CO 3	Analyze the molecular electronics or revolutionary engineering solutions.
CO 4	Analyze the Electron transport in semiconductors and nanostructures.
CO 5	Design Single modulation-doped hetero junctions.

UNIT I

Free Electron Theory & The New Ohm's Law: Why Electrons flow, Classical free electron theory, Somerfield's theory, The quantum of conductance, Coulomb blockade, Towards Ohm's law. The Elastic Resistor: Conductance of an Elastic Resistor, Elastic Resistor- Heat dissipation.

UNIT II

Materials for nano electronics: Semiconductors, Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor hetero structures, Lattice-matched and pseudo morphic hetero structures, Inorganic nano wires, Organic semiconductors, Carbon nano materials: nanotubes and fullerenes

UNIT III

Ballistic and Diffusive Transport: Ballistic and Diffusive Transfer Times, Channels for Conduction Conductivity, Conductivity: E(p) or E(k) Relations, Counting States, Drude Formula, Quantized Conductance, Electron Density -Conductivity

UNIT IV

Electron transport in semiconductors and nanostructures: Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, Fermi statistics for electrons, the density of states of electrons in nanostructures, Electron transport in nanostructures.

UNIT V

Electrons in traditional low-dimensional structures: Electrons in quantum wells: Single modulation-doped hetero junctions, Numerical analysis of a single hetero junction, Control of charge transfer, Electrons in quantum wires, Electron transport in quantum wires, Electrons in quantum dots.

Text Books:

1. Introduction to Nano Science and Technology by S.M. Lindsay.
2. Supriyo Dutta -Lessons from Nanoscience: A Lecture Note Series, World Scientific (2012).
3. Supriyo Dutta --Quantum Transport- Atom to Transistor, Cambridge University Press (2005).
4. Introduction to Nanoelectronics: Science, Nanotechnology, Engineering & Applications by Vladimir.V. Mitin.

Course Title	ANALOG AND DIGITAL CMOS VLSI DESIGN LAB				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884211	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		--	--	4	2	50	50	100
						End Exam Duration: 3Hrs		

Course Objectives:

- To learn Physical Design i.e. Stick diagrams, Lambda Design Rules and Layout making of VLSI circuits.
- To provide students with an opportunity to practice on various softwares & tools for VLSI Design and develop the mos transistors.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Write HDL code for basic as well as advanced digital integrated circuits.
CO 2	Import the logic modules into FPGA Boards.
CO 3	Synthesize Place and Route the digital ICs.
CO 4	Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.

LIST OF MAJOR EQUIPMENTS & SOFTWARE

1. FPGA Kits with
2. XILINX Simulator
3. Microwind
4. LT Spice

LIST OF EXPERIMENTS:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

Course Title	REAL TIME OPERATING SYSTEM LAB				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884212	PC	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		--	--	4	2	50	50	100
					End Exam Duration: 3Hrs		

Course Objectives:

- Able to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand an application that creates two tasks that wait on a timer whilst the main task loops.
CO 2	Analyze how to write an application to Test message queues and memory blocks.
CO 3	Design & Develop an image processing application with Linux OS on Xilinx Zynq FPGA.

List of Experiments (As per curriculum):

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task
3. Write an application that Demonstrates the interruptible ISRs(Requires timer to have higher priority than external interrupt button)
4. a).Write an application to Test message queues and memory blocks.
   b).Write an application to Test byte queues
5. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing.
6. Interfacing Programs: Write an application that creates a two task to Blinking two different LEDs at different timings
7. Write an application that creates a two task to Blinking two different LEDs at different timings
8. Write an application that creates a two task displaying two different messages in LCD display in two lines.
9. Sending messages to mailbox by one task and reading the message from mailbox by another task.
10. Sending message to PC through serial port by three different tasks on priority Basis.
11. Porting Linux and developing simple application on Xilinx Zed board
12. Developing image processing application with Linux OS on Xilinx Zynq FPGA

List of Experiments (Beyond the Syllabus):

1. Simulating a stepper-motor driver
2. Write simple applications using RTX (ARM Keil's real time operating system, RTOS).

Course Title	MINI PROJECT				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884213	PROJ	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		0	0	4	2	100	--	100
Internal Assessment								

Course Objectives:

- Acquire and apply new knowledge as needed, using appropriate learning strategies.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Demonstrate a technical knowledge of their selected project topic.
CO 2	Understand problem identification, formulation and solution.
CO 3	Design engineering solutions to complex problems utilizing a systems approach.
CO 4	Communicate with engineers and the community at large in written an oral form.
CO 5	Demonstrate the knowledge, skills and attitudes of a professional engineer.

Course Title	ENGLISH FOR RESEARCH PAPER WRITING				M. Tech. ES & VLSI II Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1870A01	Audit Course	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		2	0	0	0	40	--	40
Mid Exam Duration: 2 Hours								

Course Objectives:

- Understand that how to improve your writing skills and level of readability.
- Learn about what to write in each section.
- Understand the skills needed when writing a Title.
- Ensure the good quality of paper at very first-time submission.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand Writing skills and level of Readability.
CO 2	Analyze what to write in each section.

UNIT I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction, Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT III

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT IV

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.

M.TECH.-III- SEMESTER SYLLABUS

Course Title	IOT AND IT'S APPLICATIONS				M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884301	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the fundamentals of IOT Technologies.
- To learn different IOT protocols & IT access technologies.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Apply the Knowledge in IOT Technologies and Data management.
CO 2	Determine the values chains Perspective of M2M to IOT.
CO 3	Implement the state of the Architecture of an IOT.
CO 4	Compare IOT Applications in Industrial & real world.
CO 5	Demonstrate knowledge and understanding the security and ethical issues of an IOT.

UNIT I

FUNDAMENTALS OF IoT- Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.

IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT II

IoT PROTOCOLS- IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT

UNIT III

DESIGN AND DEVELOPMENT- Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming

UNIT IV

DATA ANALYTICS AND SUPPORTING SERVICES- Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG

UNIT V

CASE STUDIES/INDUSTRIAL APPLICATIONS: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / IntelGalileo/ARM Cortex/ Arduino)

Text Books:

1.IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, DavidHanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017

Reference Books:

1. Arshdeep Bahga, Vijay Madisetti "Internet of Things" – A hands-on approach, , Universities Press, 2015
2. Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley "The Internet of Things" – Key applications and Protocols, , 2012 (for Unit 2).
3. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence",Jan Ho¨ ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.

Course Title	HARDWARE SOFTWARE CO DESIGN				M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1884302	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To design and analyze Hardware-Software Code design Methodology.
- To Understand the importance of system level specification languages.
- To design and compiler development environment.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Explain About the Hardware-Software Code design Methodology
CO 2	Analyze how to select a target architecture and how a prototype is built
CO 3	Explain how emulation of a prototype is done.
CO 4	Briefviewaboutcompilationtechnologiesandcompilerdevelopmentenvironment.
CO 5	Understand the importance of system level specification languages and multi-language co-simulation.

UNIT I

Co-Design Issues: Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms: Hardware software synthesis algorithms, hardware–software partitioning distributed system co-synthesis

UNIT II

Prototyping and Emulation

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification:

Design, co-design, the co design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, Interface verification

UNIT V

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages. Languages for System-Level Specification and Design-II Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system

Text Books:

1. Wayne Wolf -Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, – 2009,Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, KluwerAcademicPublishers

Course Title	ARTIFICIAL INTELLIGENCE					M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884303	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To Understand the concept of Artificial Intelligence
- To Understanding reasoning and fuzzy logic for artificial intelligence
- To Analyze Symbolic Reasoning Under Uncertainty

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the concept of Artificial Intelligence.
CO 2	Explain the search techniques and knowledge representation issues.
CO 3	Understanding reasoning and fuzzy logic for artificial intelligence.
CO 4	Analyze Symbolic Reasoning Under Uncertainty.
CO 5	Understanding game playing and natural language processing.

UNIT I

What is AI (Artificial Intelligence)? : The AI Problems, The Underlying Assumption, What are Techniques, The Level Of The Model, Criteria For Success, Some General References, One Final Word Problems, State Space Search & Heuristic Search Techniques: Defining The Problems As A State Space Search, Production Systems, Production Characteristics, Production System Characteristics, And Issues In The Design Of Search Programs, Additional Problems. Generate-And-Test, Hill Climbing, Best-First Search, Problem Reduction, Constraint Satisfaction, Means-Ends Analysis.

UNIT II

Knowledge Representation Issues: Representations and Mappings, Approaches To Knowledge Representation. Using Predicate Logic: Representation Simple Facts In Logic, Representing Instance And Isa Relationships, Computable Functions And Predicates, Resolution. Representing Knowledge Using Rules: Procedural versus Declarative Knowledge, Logic Programming, and Forward Versus Backward Reasoning.

UNIT III

Symbolic Reasoning Under Uncertainty: Introduction To Nomonotonic Reasoning, Logics For Non-monotonic Reasoning. Statistical Reasoning: Probability And Bays‟ Theorem, Certainty Factors And Rule-Base Systems, Bayesian Networks, Dempster Shafer Theory. Fuzzy Logic. Weak Slot-and-Filler Structures: Semantic Nets, Frames. Strong Slot-and-Filler Structures: Conceptual Dependency, Scripts, CYC.

UNIT IV

Game Playing: Overview, And Example Domain: Overview, Mini Max, Alpha-Beta Cut-off, Refinements, Iterative deepening, The Blocks World, Components Of A Planning System, Goal Stack Planning, Nonlinear Planning Using Constraint Posting, Hierarchical Planning, Reactive Systems, Other Planning Techniques. Understanding: What understands? What makes ithard?As constraint satisfaction

UNIT V

Natural Language Processing: Introduction, Syntactic Processing, Semantic Analysis, Semantic Analysis, Discourse And Pragmatic Processing, Spell Checking Connectionist Models: Introduction: Hopfield Network, Learning In Neural Network, Application Of Neural Networks, Recurrent Networks, Distributed Representations, Connectionist AI And Symbolic AI

Text Books:

1. ElaineRichandKevinKnight“ArtificialIntelligence”,2ndEdition,Tata Mcgraw-Hill,2005.

2. Stuart Russel and Peter Norvig,“ArtificialIntelligence:AModernApproach”,3rdEdition,PrenticeHall, 2009

Course Title	RFIC DESIGN					M. Tech. ES & VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1884304	PE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To design various constituents' blocks of RF receiver front end
- To Understand the design bottlenecks specific to RF IC design
- To Specify noise and interference performance metrics like noise figure

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the design bottlenecks specific to RF IC design, linearity related issues, ISI.
CO 2	Identify noise sources, develop noise models for the devices and systems.
CO 3	Specify noise and interference performance metrics like noise figure, IIP3 and different matching criteria.
CO 4	Comprehend different multiple access techniques, wireless standards.
CO 5	Design various constituents' blocks of RF receiver front end.

UNIT I

INTRODUCTION TO RF AND WIRELESS TECHNOLOGY: Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology.

UNIT II

BASIC CONCEPTS IN RF DESIGN: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, passive impedance transformation.

UNIT III

MULTIPLE ACCESS: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. TRANSCEIVER ARCHITECTURES: General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies.

UNIT IV

AMPLIFIERS, MIXERS AND OSCILLATORS: LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers.

UNIT V

POWER AMPLIFIERS: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques.

Text Books:

1. BehzadRazavi, RF Microelectronics Prentice Hall of India, 2001

2. Thomas H. Lee, The Design of CMOS Radio Integrated Circuits, Cambridge University Press.

3. B. Leunge, VLSI for Wireless Communication, Personal Education Electronics and VLSI series, Pearson Education, 2002

OPEN ELECTIVES

1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Composite Materials
5. Cost Management of Engineering Projects
6. Waste to Energy

Course Title	BUSINESS ANALYTICS				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1871305	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- Understand the role of business analytics within an organization.
- Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
- To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
- To become familiar with processes needed to develop, report, and analyze business data.Use decision-making tools/Operations research techniques.
- Mange business process using analytical and management tools.
- Analyze and solve problems from different industries such as manufacturing, service, retail, software, banking and finance, sports, pharmaceutical, aerospace etc.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Students will demonstrate knowledge of data analytics.
CO 2	Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
CO 3	Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making
CO 4	Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT I

Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organisation, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

UNIT II

Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

UNIT III

Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

UNIT IV

Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models.

Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

UNIT V

Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making. Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education

Course Title	INDUSTRIAL SAFETY				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1871306	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To Understand the Fundamentals of maintenance engineering.
- To Understand the Fire prevention and firefighting, equipment and methods.
- Analyze the fault tracing-concept and importance.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To Understand the Fundamentals of maintenance engineering
CO 2	To Understand the Fire prevention and firefighting, equipment and methods
CO 3	Analyze the fault tracing-concept and importance
CO 4	Analyze the Steps/procedure for periodic and preventive maintenance

UNIT I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler,

Electrical motors, Types of faults in machine tools and their general causes

UNIT V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference Books:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication

Course Title	OPERATION RESEARCH					M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
1871307	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs			

Course Objectives:

- To understand the dynamic programming to solve problems of discreet and continuous variables.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Able to apply the dynamic programming to solve problems of discreet and continuous variables.
CO 2	Able to apply the concept of non-linear programming
CO 3	Able to carry out sensitivity analysis
CO 4	Able to model the real world problem and simulate it

UNIT I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

UNIT II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

UNIT III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

UNIT IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References Books:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010

Course Title	COMPOSITE MATERIALS				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1871308	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the characteristics of Composite materials.
- To understand Manufacturing of Metal Matrix Composites.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	understand the Classification and characteristics of Composite materials
CO 2	Analyze the Manufacturing of Ceramic Matrix Composites
CO 3	Analyze the Manufacturing of Polymer Matrix Composites

UNIT I

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT III

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT IV

Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books:

1. R.W.Cahn – VCH "Material Science and Technology" – Vol 13 – Composites, West Germany.
2. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY "Materials Science and Engineering", An introduction., Indian edition, 2007.

Reference Books:

1. Hand Book of Composite Materials-ed-Lubin.
2. Composite Materials – K.K.Chawla.
3. Composite Materials Science and Applications – Deborah D.L. Chung.
4. Composite Materials Design and Applications – Danial Gay, Suong V. Hoa, and Stephen W. Tasi.

Course Title	COST MANAGEMENT OF ENGINEERING PROJECTS				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1871309	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the Overview of the Strategic Cost Management Process.
- To understand Cost Behavior and Profit Planning Marginal Costing.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	To understand the Overview of the Strategic Cost Management Process.
CO 2	Analyze various stages of project execution.
CO 3	Evaluate Bar charts and Network diagram.

UNIT I

Introduction and Overview of the Strategic Cost Management Process: Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process

UNIT III

Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector.

UNIT IV

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

Reference Books:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

Course Title	WASTE TO ENERGY				M. Tech. ES &VLSI III Sem		
Course Code	Category	Hours/Week			Credits	Maximum Marks	
1871310	OE	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		3	--	--	3	40	60	100
Mid Exam Duration: 2Hrs					End Exam Duration: 3Hrs		

Course Objectives:

- To understand the Classification of waste as fuel – Agro based, Forest residue Industrial waste - MSW – Conversion devices – Incinerators

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Understand the Classification of waste as fuel
CO 2	Explain the Properties of biogas
CO 3	Design and constructional features - Biomass resources and their classification - Biomass conversion processes

UNIT I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Reference Books:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Course Title	DISSERTATION PHASE-I				R18- M.Tech DECS III Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884311	MAJOR PROJECT	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		0	0	20	10	100	--	100
Internal Assessment								

Course Objectives:

- Acquire and apply new knowledge as needed, using appropriate learning strategies.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Demonstrate a technical knowledge of their selected project topic.
CO 2	Understand problem identification, formulation and solution.
CO 3	Communicate with engineers and the community at large in written an oral form.
CO 4	Demonstrate the knowledge, skills and attitudes of a professional engineer.

M.TECH.-IV- SEMESTER SYLLABUS

Course Title	DISSERTATION PHASE-II				R18- M.Tech DECS IV Sem		
Course Code	Category	Hours/Week		Credits	Maximum Marks		
1884401	MAJOR PROJECT	L	T	P	C	Continuous Internal Assessment	End Exams	Total
		0	0	32	16	50	50	100
					External Assessment			

Course Objectives:

- Acquire and apply new knowledge as needed, using appropriate learning strategies.

Course Outcomes: On successful completion of this course, the students will be able to

CO 1	Demonstrate a technical knowledge of their selected project topic.
CO 2	Design engineering solutions to complex problems utilizing a systems approach.
CO 3	Communicate with engineers and the community at large in written an oral form.
CO 4	Demonstrate the knowledge, skills and attitudes of a professional engineer.